

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl.No.: 10/712,736
Appellant: Cheung et al
Filed: 11/12/2003
TC/AU: 2182
Examiner: Nguyen

Confirmation No.: 8891

Docket: TI-32389.1
Cust.No.: 23494

SUBSTITUTE APPEAL BRIEF

Commissioner for Patents
P.O.Box 1450
Alexandria VA 22313-1450

Sir:

In response to the Notice of Non-Compliant Appeal Brief mailed 07/20/2006, appellants attach the following sheets which contain the Rule 41.37 items of appellants' substitute Appeal Brief. The Commissioner is hereby authorized to charge any necessary fees to the deposit account of Texas Instruments Incorporated, account No. 20-0668.

Respectfully submitted,

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Rule 41.37(c)(1)(i) Real party of interest

Texas Instruments Incorporated owns the application.

Rule 41.37(c)(1)(ii) Related appeals and interferences

There are no related dispositive appeals or interferences.

Rule 41.37(c)(1)(iii) Status of claims

Claims 7-11 and 13-20 are pending in the application with claims 13-20 withdrawn from consideration and claims 7-11 finally rejected. This appeal involves the finally rejected claims.

Rule 41.37(c)(1)(iv) Status of amendments

There is no claim amendment after final rejection.

Rule 41.37(c)(1)(v) Summary of claimed subject matter

The claim 7 invention (only claim argued) provides a serial peripheral interface (SPI) for a microcontroller which uses a FIFO with separate SPI and microcontroller transmit/receive pointers and difference counters for handling microcontroller communications with peripherals; the FIFO is part of the microcontroller's memory and is accessed by the SPI through the microcontroller's DMA using cycle stealing, thereby not loading the microcontroller. Fig.1 shows SPI 108 between the microcontroller bus interface 104 (plus DMA 112) and peripherals 101; the FIFO is in CPU SRAM 106. Fig.2B heuristically illustrates FIFO 208 as a circle of 16 memory locations with SPI pointers SPITxp for transmit and SPIrxp for receive plus microcontroller pointers CPUtxp for transmit and CPUrxp for receive; TXcnt is the transmit difference counter and RXcnt is the receive difference counter. Application paragraphs [0026] and [0048] describe the cycle stealing, and paragraphs [0028] to [0033] describe the operation of the FIFO and pointers and counters for communications of the microcontroller with peripherals. The SPI essentially

buffers microcontroller communications using part of the microcontroller's memory but without loading the microcontroller.

Rule 41.37(c)(1)(vi) Grounds of rejection to be reviewed on appeal

The grounds of rejection to be reviewed on appeal are:

(1) Claims 7-11 were rejected as unpatentable over the Hill reference in view of the Sowell reference.

Rule 41.37(c)(1)(vii) Arguments

(1) Claims 7-11 were rejected as unpatentable over Hill in view of Sowell.

Appellants reply that Hill does not disclose or suggest the presently claimed invention including the SPI being further configured to communicate with DMA module and the bus interface for providing cycle stealing (claim 7, last clause). Appellants agree with the Examiner (as evidenced by page 4 of the Office Action) that Hill does not disclose the SPI for providing cycle stealing.

It is respectfully submitted that Sowell also does not disclose or suggest the presently claimed invention including the SPI being further configured to communicate with the DMA module and the bus interface for providing cycle stealing (claim 7, last clause). The Board's attention is directed to column 3, lines 5-10 of Sowell. Here, Sowell discloses that the direct memory access DMA provides a fast means for retrieving and placing data that is required for the HDLC block. The DMA is generally used in a "cycle stealing mode" which provides an efficient means of data movement. Sowell or any prior art reference applied by the Examiner does not disclose a SPI having cycle stealing.

Rule 41.37(c)(1)(viii) Claims appendix

7. A serial peripheral interface (SPI) for use with a microcontroller and configured for increasing the rate of data communications, wherein the SPI module comprises:

- a plurality of hardware pointers to memory locations in a FIFO buffer;
 - at least one hardware pointer counter; and
 - a hardware logic device; wherein the hardware logic device is configured to communicate with a bus interface and to utilize the FIFO buffer for intermediate storage of data being transmitted from and received to the CPU,
- wherein the SPI is further configured to communicate with a DMA module and the bus interface for providing cycle stealing.

8. The SPI of claim 7 wherein the plurality of hardware pointers are configured to provide at least one of a CPU transmitter pointer signal, a CPU receiver pointer signal, a SPI transmitter pointer signal and a SPI receiver pointer signal.

9. The SPI of claim 7 the SPI module further comprising a transmitter buffer and a receiver buffer;

wherein the transmitter buffer is configured to transmit data from the FIFO buffer, and wherein the receiver buffer is configured to transmit data to the FIFO buffer.

10. The SPI of claim 7 the SPI module further configured to operate as one of a master device and a slave device.

11. The SPI of claim 7 the SPI module further configured to provide a data register chip select signal to the bus interface.

Rule 41.37(c)(1)(ix) Evidence appendix

none

Rule 41.37(c)(1)(x) Related proceedings appendix

none